REMARKS/ARGUMENTS

The Applicants have carefully considered this Application in connection with the Examiner's Action and respectfully request reconsideration of this Application in view of the following remarks.

The Applicants originally submitted Claims 1-42 in the Application. In previous responses, the Applicants cancelled Claims 8 and 18 without prejudice or disclaimer, and submitted Claims 43-44 for examination. Claims 21 and 31 are presently amended to address an objection of the Examiner. Accordingly, Claims 1-7, 9-17, 19, 20, 43 and 44 are currently pending in the Application.

I. Formal Matters

The Applicants note the objection of the Examiner to Claims 21 and 31, and have amended these claims to recite "a plurality of programmable ..." The Applicants respectfully request that the Examiner now withdraw these objections.

The Applicants again note with appreciation that the Examiner has indicated that Claims 21-42 are allowed.

II. Rejection of Claims 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. § 103

The Examiner has rejected Claims 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6.807,581 to Starr, *et al* ("Starr") in view of U.S. Patent No. 6,792,502 to Pandya, *et al* ("Pandya"). The Applicants respectfully disagree with this rejection, and request that these claims be allowed to issue.

Amended Claim 1 is directed to a media access controller and a programmable logic core block (MP-block) of a field programmable network application specific integrated circuit (ASIC), comprising a media access controller configured to transmit and receive network data; and a programmable logic core *having an array of arithmetic logic units* dynamically configurable to implement a plurality of application level functions capable of generating meta-data, said programmable logic core configured to interface with said media access controller and implement at least one of said plurality of application level functions. (Emphasis added.)

Starr is generally directed to an interface device, such as an intelligent network interface card (NIC), for a local host that provides hardware and processing mechanisms for accelerating data transfers between a network and a storage unit, while control of the data transfers remains with the host. The interface device includes hardware circuitry for purportedly processing network packet headers, and can use a dedicated fast-path for data transfer between the network and the storage unit, the fast-path set up by the host. The host CPU and protocol stack avoid protocol processing for data transfer over the fast-path, releasing host bus bandwidth from demands of the network and storage subsystem. (*See* col. 3, lines 8-19.)

Pandya is generally directed to content addressable memory (CAM) architecture for purportedly efficient accessing of data in a data processing system. The CAM architecture includes various new data fields within the CAM data row entries and includes circuitry for accessing the CAM data. (*See* col. 2, lines 56-59.)

The Examiner states that Starr "fails to teach an array of arithmetic logic units." (See Examiner's Action, page 3.) The Applicants agree with the Examiner.

The Examiner then cites Pandya. The Examiner states that:

However, Pandya discloses a processor 310 comprising a *plurality* arithmetic logic units ALUs (fig. 9, col. 12 lines 19-24). This, it would have been obvious to a person of ordinary skill in the art to arrange for a *plurality* of arithmetic logic units ALUs as taught by Pandya in Starrs system to speed up or/and enhance the processor functions. (*See* Examiner's Action, page 3; emphasis added.)

Column 12, lines 19-24 of Pandya, read as follows:

FIG. 8 illustrates *at least one arithmetic logic unit (ALU) 460* which represents one or more integer units[,] one or more floating point units, and/or one or more other arithmetic logic units. Additional ALUs is (*sic.*) may be a multiply accumulator, a barrel shifter[,] an algebraic function processor, or other ALU that may be used within modern processors. (Emphasis added.)

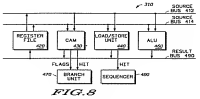

FIG. 8

However, the Applicants respectfully contend that Pandya does not cure the deficiencies of Starr, Since Pandya fails to teach an array of arithmetic logic units for two reasons, as will be detailed below.

The first reason is that Pandya does not disclose a *plurality* of ALUs, as characterized by the Examiner. Instead, Pandyan refers to "at least one" ALU, and only discloses one ALU in FIG. 8. The Applicants respectfully contend that the above discussion and disclosure does not disclose a "plurality" of ALUs as proposed by the Examiner.

Secondly, assuming, *arguendo,* that Pandya *does* disclose a "plurality of ALUs", these are not the ALUs as claimed in independent Claim 1. Claim 1 recites "... a programmable logic core *having an array of arithmetic logic units* dynamically configurable to implement a plurality of application level functions..." A proposed plurality of ALUs, as proposed by the Examiner, is simply

not an "array" of arithmetic logic units, as claimed in Claim 1.

Furthermore, an array of arithmetic logic units have a physical relationship to one another that is not disclosed in a purported "plurality "of ALUs of Pandya. For instance, in the present Application:

> In one advantageous embodiment, an array of dynamically configurable arithmetic logic units contains an array of 16 (4x4) Hex blocks. A Hex block is generally understood as the smallest geometric region used to build larger arrays. As such, arrays are commonly quoted in terms of Hex blocks, wherein each Hex block contains 16 quad blocks, and each quad block contains 4 register transfer level (RTL) configurable arithmetic logic units. (*See* paragraph [0028].)

Arrays of ALUs, such as discussed in the Application, are simply not disclosed in Pandya. Starr, individually or in combination with Pandya, fails to teach or suggest the invention recited in independent Claim 1 and its dependent claims, when considered as a whole. For similar reasons, Pandya fails to teach or suggest the invention recited in independent Claim 11 and its dependent claims, when considered as a whole. Claims 1-7, 9-17, 19, 20, 43 and 44 are therefore not obvious in view of Starr and Pandya.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. §103(a). Accordingly, the Applicants respectfully request that the Examiner withdraw the rejection of Claims 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. § 103(a) and allow issuance thereof.

III. Conclusion

In view of the foregoing remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for all of the pending Claims 1-7, 9-17, 19, 20, 43 and 44.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 12-2252.

Respectfully submitted,

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